UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,430	10/31/2000	James B. Cho	TI-30961	2977

		EXAMINER
7590	09/29/2004	DUONG, FRANK

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ART UNIT	PAPER NUMBER
2666	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/703,430	CHO ET AL.
	Examiner	Art Unit	
	Frank Duong	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _31 October 2000_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _6/29/01_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to the communication dated 10/31/2000. Claims 1-

30 are pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed 06/29/01 complies with the provisions of

37 CFR 1.97, 1.98 and MPEP § 609. It has been considered and placed in the

application file.

Claim Objections

3. Claim 23 is objected to because of the following informalities:

Lines 3-4, "said determining" should read --said nodes determining--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Stepheson,

Jr. et al (USP 5,081,654) (hereinafter "Stephenson").

Regarding **claim 1**, in accordance with Stephenson reference entirety,

Stephenson discloses a bit rate detection circuit (Fig. 3), comprising:

a plurality of shift registers (24, 25, 25', 28, 28', 28", 32 and 34) adapted to

serially shift in bits of data (22) having a data frequency (*col. 5, line 28; 55.52 Mbps*)

from a first transceiver (*not shown; inherent depicted as source of signal 22 in Fig. 3*),

said shift registers being clocked at a first predetermined rate (*col. 5, lines 59-62*); and

logic circuitry ((*25, 25', 28 and 28') and (32, 34 and 40)*) responsively coupled to

(DATA#1, DATA#2, DATA#3) said shift registers (24) providing an output signal (*Fig. 3;*

output of 40 or Fig. 4; 49) indicative of the data frequency (STS-3).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales

discussed above), Stephenson further discloses wherein said first predetermined rate is

the highest possible data rate that the incoming data frequency can be (*col. 5, lines 66-*

68).

Regarding **claim 3**, in addition to features recited in base claim 1 (see rationales

discussed above), Stephenson further discloses wherein said logic circuitry is coupled

to node (32 and 34) defines between said shift registers (24) (*see Fig. 3 for details of*

connections).

Regarding **claim 4**, in addition to features recited in base claim 3 (see rationales

discussed above), Stephenson further discloses wherein said logic circuitry comprises a

first logic set (*Fig. 4; A1 Detectors 32*) and a second logic set (*Fig. 4; A2 Detectors 34*)

each providing an output signal (*Fig. 4; 37 and 43*), said first logic set being coupled to a

first set of said nodes between said shift registers, and said second logic set being

coupled to a second set of said nodes between said shift registers (see Fig. 4 for details

of connections).

Regarding **claim 5**, in addition to features recited in base claim 4 (see rationales

discussed above), Stephenson further discloses wherein said first logic set (32)

determines if said incoming data frequency is a first predetermined frequency (A1 byte),

and said second logic set (34) determines if said incoming data frequency is a second

predetermined frequency (A2) being less than said first predetermined frequency (*col. 9,*

lines 45-46 and thereinafter).

Regarding **claim 6**, in addition to features recited in base claim 5 (see rationales

discussed above), Stephenson further discloses wherein said first predetermined

frequency (STS-3) is a multiple of said second predetermined frequency (STS-1) (col. 5,

lines 26-29).

Regarding **claim 7**, in addition to features recited in base claim 4 (see rationales

discussed above), Stephenson further discloses output logic circuitry (40) responsively

coupled to said first logic set (32) and said second logic set (34), said output logic

circuitry (40) providing said output signal (49) indicative of the data frequency (*col. 7,*

line 41 to col. 8, line 4).

Regarding **claim 8**, in addition to features recited in base claim 4 (see rationales

discussed above), Stephenson further discloses a third logic set (Fig. 5; 48) coupled to

a third set of said nodes (Fig. 5; 39 and 47) being different than said first and second

sets of nodes (*see Fig. 5 for details of connections*).

Regarding **claim 9**, in addition to features recited in base claim 8 (see rationales discussed above), Stephenson further discloses wherein said third logic set (48) determines if said incoming data frequency is a third predetermined frequency being less than said second predetermined frequency (*col. 7, lines 54-59*).

Regarding **claim 10**, in addition to features recited in base claim 9 (see rationales discussed above), Stephenson further discloses wherein said first predetermined frequency is in multiple of said third predetermined frequency (*col. 7, line 41 to col. 8, line 4*).

Regarding **claim 11**, in addition to features recited in base claim 10 (see rationales discussed above), Stephenson further discloses wherein said third predetermined frequency is also a multiple of said second predetermined frequency (*col. 7, line 41 to col. 8, line 4*).

Regarding **claim 12**, in addition to features recited in base claim 1 (see rationales discussed above), Stephenson further discloses a communications transceiver module responsively coupled to said logic circuitry output signal and adapted to transmit data back to said first transceiver at said incoming data frequency (*not shown; Stephenson's reference only shows the receiving side of the SONET transceiver. However, it is inherent there is transmitting side of the SONET transceiver accompanying the transceiver to encompass the claimed limitation*).

Regarding **claim 13**, in addition to features recited in base claim 1 (see rationales discussed above), Stephenson further discloses wherein said logic circuitry includes a single clock operating at a first frequency (*Fig. 3; 39MHz*).

Regarding **claim 14**, in addition to features recited in base claim 1 (see

rationales discussed above), Stephenson further discloses wherein said logic circuit

provides said output signal (DATA#1, DATA#2 and DATA#3) as a function of framing

data (A1 and A2) clocked into said shift registers (24, 25, 25', 28, 28', 28", 32 and 34)).

Regarding **claim 15**, in addition to features recited in base claim 14 (see

rationales discussed above), Stephenson further discloses wherein said framing data is

A1 and A2 SONET framing bytes (*Fig. 2 and col. 4, lines 22-28*).

Regarding **claim 16**, in accordance with Stephenson reference entirety,

Stephenson discloses a data transceiver (*Figs. 3-4, col. 5, line 55 to col. 10, line 2*),

comprising:

a data receiver circuit (*not shown; inherent as depicted in Fig. 3 as source of*

signal 22);

logic circuitry (*Fig. 3; 24, 25, 25', 28, 28', 28", 32, 34 and 40*) responsively

coupled to said receiver circuit determining a data rate of data received by said data

receiver, said logic circuit including and operating off a single clock operating at a first

predetermined frequency (39 MHz); and

a data transmitter (Fig. 3; 36) responsively coupled to said logic circuitry and

adapted to transmit data at a data rate as a function of said output signal (38) (*see*

Figure 3 for connections).

Regarding **claim 17**, in addition to features recited in base claim 16 (see

rationales discussed above), Stephenson further discloses wherein said logic circuitry

comprises:

a plurality of shift registers (24) adapted to serially shift in data having a data

frequency from a first transceiver (not shown; source of signal 22) (*col. 5, lines 55-66*),

said shift registers being clocked at a first predetermined rate (155.52 Mbps) (*col. 5,*

lines 26-29); and

logic circuitry (25) responsively coupled to said shift registers (24) providing an

output signal (output at 25, 25' and 25") indicative of the incoming data frequency (*col.*

5, lines 65-66)

Regarding **claim 18**, in addition to features recited in base claim 17 (see

rationales discussed above), Stephenson further discloses wherein said first

predetermined rate is the highest possible data rate that the incoming data frequency

can be (*col. 5, lines 66-68*).

Regarding **claim 19**, in addition to features recited in base claim 17 (see

rationales discussed above), Stephenson further discloses wherein said logic circuitry is

coupled to nodes defined between said shift registers (*see Fig. 3 for details of*

connections).

Regarding **claim 20**, in addition to features recited in base claim 19 (see

rationales discussed above), Stephenson further discloses wherein said logic circuitry

comprises a first logic set (Fig. 4; 32) and a second logic set (Fig. 4; 34) each providing

an output signal (Fig. 4; 37 and 43), said first logic set (32) being coupled to a first set of

said nodes (28' and 28") defined between said shift registers (24), and said second

logic set (34) being coupled to a second set of said nodes (28 and 28') defined between

said shift registers (24) (*see Fig. 4 for detail connections*).

Regarding **claim 21**, in accordance with Stephenson reference entirety,

Stephenson discloses a method of detecting a bit-rate of data (*Figs. 3-4, col. 5, line 55*

to col. 10, line 2) incoming to a receiver (not shown; inherent as source as signal 22),

comprising the steps of:

a) clocking said incoming bit data (22) at a first frequency into a plurality of shift

registers (24, 25, 25', 28, 28', 28", 32 and 34) having a node (Fig. 3; DATA #1

connected to 34 and DATA#2 and DATA#3 connected to 32) between each said shift

register (24, 25, 25', 28, 28', 28", 32 and 34); and

b) analyzing (32 and 34) data at a plurality of said nodes to determine the bit-rate

of said incoming bit data (*col. 6, lines 24-36 and thereinafter*).

Regarding **claim 22**, in addition to features recited in base claim 21 (see

rationales discussed above), Stephenson further discloses wherein said first frequency

is the maximum possible data bit-rate of said incoming bit data (*col. 5, lines 66-68*).

Regarding **claim 23**, in addition to features recited in base claim 22 (see

rationales discussed above), Stephenson further discloses wherein logic circuitry (20)

analyzes said bit data, said logic circuitry (20) having a first logic set (32) coupled to a

first set of said nodes (28' and 28") determining if said data bit-rate could be a first data

rate (F6 detector), and a second logic set (34) coupled to a second set of said nodes

(28 and 28') determining if said data bit-rate could be a second data rate being less than

said first data rate (*col. 6, line 24 to col. 7, line 41, Stephenson discusses the functions

of A1 and A2 detectors 32 and 34*).

Regarding **claim 24**, in addition to features recited in base claim 23 (see rationales discussed above), Stephenson further discloses wherein said first data rate is said first frequency (STS-3), and said first data rate is also a multiple of said second data rate (STS-1) (*col. 5, lines 26-29*).

Regarding **claim 25**, in addition to features recited in base claim 21 (see rationales discussed above), Stephenson further discloses responsively transmitting data from a transmitter (Fig. 3; 36) at a data rate being said determined incoming data bit-rate (*col. 7, line 60 to col. 8, line 4*).

Regarding **claim 26**, in addition to features recited in base claim 21 (see rationales discussed above), Stephenson further discloses wherein frame data is said analyzed data in said step b) (*col. 6, lines 24-36 and thereinafter*).

Regarding **claim 27**, in addition to features recited in base claim 26 (see rationales discussed above), Stephenson further discloses where in said frame data is a A1 and A2 SONET framing byte (*col. 6, lines 24-36 and thereinafter*).

Regarding **claim 28**, in accordance with Stephenson reference entirety, Stephenson discloses a bit-rate detection circuit (*Figs. 3-4 and col. 4, line 49 to col. 10, line 2*), comprising:

a plurality of shift registers (*Fig. 3; 25, 25', 28, 28', 28"*) adapted to shift in bits of data having a data rate in parallel from a first transceiver (24), said shift registers being clocked at a predetermined clock rate (39) (*col. 6, lines 9-65*); and

logic circuitry (32 and 34) responsively coupled to said shift registers providing an output signal (Fig. 4; 49) indicative of the data rate (*col. 7, line 60 to col. 8,line 4*).

Regarding **claim 29**, in addition to features recited in base claim 28 (see
rationales discussed above), Stephenson further discloses wherein said clock rate (39
MHz) is less than the maximum data rate (155.52 Mbps) (*col. 5, line 55 to col. 6, line 8*).

Regarding **claim 30**, in addition to features recited in base claim 29 (see
rationales discussed above), Stephenson further discloses wherein said data rate is a
multiple of said clock rate (*col. 5, line 55 to col. 6, line 8*).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to
applicant's disclosure.

Chang et al (USP 6,526,109).

Johansen (USP 6,631,144).

Marmur (USP 6,466,886).

Belot et al, A 3.3-V Power Adaptiver 1244/622/155 Mbit/s Transceiver for ATM,
SONET/SDH, IEEE pages 1047-1058, 1998.

Seo et al, A 3V Low Power 156/622/1244 Mbps CMOS Parallel Clock and Data
Recovery Circuit for Optical Communications, IEICE, pages 1720-1727, 2000.

6. Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Frank Duong whose telephone number is (571) 272-
3164. The examiner can normally be reached on 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Frank Duong
Examiner
Art Unit 2666

September 27, 2004